

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Leonard Forbes et al.

STRAINED SEMICONDUCTOR BY FULL WAFER BONDING

Docket No.:

1303.109US1

Serial No.: 10/623788

Filed:

July 21, 2003

Due Date: N/A

Examiner:

Unknown

Group Art Unit: 2811

Ms Amendment

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

We are transmitting herewith the following attached items (as indicated with an "X"):

- A return postcard.
- A Communication Concerning Related Applications (2 pgs.).
- An Information Disclosure Statement (2 pgs.), Form 1449 (7 pgs.), and copies of 73 cited documents.

If not provided for in a separate paper filed herewith, Please consider this a PETITION FOR EXTENSION OF TIME for sufficient number of months to enter these papers and please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

Customer Number 21186

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this <u>loru</u> day of May, 2004.

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

(GENERAL)

PATENT

S/N 10/623788
IN THE UNKED STATES PATENT AND TRADEMARK OFFICE

Applicant:

Leonard Ferbes et al.

Examiner: Unknown

Serial No.:

10/623788

Group Art Unit: 2811

Filed:

July 21, 2003

Docket: 1303.109US1

Title:

STRAINED SEMICONDUCTOR BY FULL WAFER BONDING

COMMUNICATION CONCERNING RELATED APPLICATION(S)

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Applicants would like to bring to the Examiner's attention the following related application(s) in the above-identified patent application:

<u>Serial/Patent No.</u> 10/052952	Filing Date January 17, 2002	Attorney Docket 1303.034US1	Title THREE-DIMENSIONAL PHOTONIC CRYSTAL WAVEGUIDE STRUCTURE AND METHOD
10/382246	March 5, 2003	1303.086US1	CELLULAR MATERIALS FORMED USING SURFACE TRANSFORMATION
10/379749	March 5, 2003	1303.089US1	MICRO-MECHANICALLY STRAINED SEMICONDUCTOR FILM
10/425797	April 29, 2003	1303.093US1	LOCALIZED STRAINED SEMICONDUCTOR ON INSULATOR
10/431134	May 7, 2003	1303.094US1	STRAINED Si/SiGe STRUCTURES BY ION IMPLANTATION
10/425484	April 29, 2003	1303.095US1	STRAINED SEMICONDUCTOR BY WAFER BONDING WITH MISORIENTATION
10/443340	May 21, 2003	1303.099US1	ULTRA-THIN SEMICONDUCTORS BONDED ON GLASS SUBSTRATES
10/431137	May 7, 2003	1303.100US1	MICROMECHANICAL STRAINED SEMICONDUCTOR BY WAFER BONDING
10/634174	August 5, 2003	1303.102US1	STRAINED Si/SiGe/SOI ISLANDS AND PROCESSES OF MAKING SAME



COMMUNICATION CONCERNING RELATED APPLICATIONS

Serial Number: 10/623788 Filing Date: July 21, 2003

Title: STRAINED SEMICONDUCTOR BY FULL WAFER BONDING

Page 2

Dkt: 1303.109US1

THE STRAINED SEMIN	CONDUCTOR BITO	EL WIN EN BONDING	
10/443337	May 21, 2003	1303.103US1	GETTERING OF SILICON ON INSULATOR USING RELAXED SILICON GERMANIUM EPITAXIAL PROXIMITY LAYERS
10/443339	May 21, 2003	1303.104US1	WAFER GETTERING USING RELAXED SILICON GERMANIUM EPITAXIAL PROXIMITY LAYERS
10/623794	July 21, 2003	1303.108US1	GETTERING USING VOIDS FORMED BY SURFACE TRANSFORMATION
09/855532	May 16, 2001		METHOD OF FORMING MIRRORS BY SURFACE TRANSFORMATION OF EMPTY SPACES IN SOLID STATE MATERIALS
10/118350	April 14, 2004		METHOD OF FORMING SPATIAL REGIONS OF A SECOND MATERIAL IN A FIRST MATERIAL
10/093332	April 14, 2004		METHOD AND APPARATUS FOR PACKAGING SEMICONDUCTOR DEVICES

Respectfully submitted,

LEONARD FORBES ET AL.

By Applicants' Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

P.O. Box 2938

Minneapolis, MN 55402

(612) 373-6960

Date 5-10-04

Reg. No. 38,377

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 10711 day of May, 2004.



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Leonard Forbes et al.

Examiner:

Unknown

Serial No.:

10/623788

Group Art Unit:

2811

Filed:

July 21, 2003

Docket:

1303.109US1

Title:

STRAINED SEMICONDUCTOR BY FULL WAFER BONDING

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 et. seq., the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicants respectfully request that this Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicants request that a copy of the 1449 form, initialed as being considered by the Examiner, be returned to the Applicants with the next official communication.

Pursuant to 37 C.F.R. §1.97(b), it is believed that no fee or statement is required with the Information Disclosure Statement. However, if an Office Action on the merits has been mailed, the Commissioner is hereby authorized to charge the required fees to Deposit Account No. 19-0743 in order to have this Information Disclosure Statement considered.

The Examiner is invited to contact the Applicants' Representative at the below-listed telephone number if there are any questions regarding this communication.

The present application is either a U.S. national patent application filed after June 30, 2003 or an international application that entered the national stage under 35 U.S.C. § 371 after June 30, 2003. Thus, Applicant believes that the U.S. Patent & Trademark Office has waived the requirement under 37 C.F.R. 1.98 (a)(2)(i) for submitting a copy of each cited U.S. patent and each U.S. patent application publication. The waiver is provided in a pre-OG notice from the U.S. Patent & Trademark Office entitled "Information Disclosure Statements May Be Filed Without Copies of U.S. Patents and Published Applications in Patent Applications filed after

Filing Date: July 21, 2003

Title: STRAINED SEMICONDUCTOR BY FULL WAFER BONDING

Dkt: 1303.109US1

June 30, 2003" and dated July 11, 2003. Applicant acknowledges the requirement to submit copies of foreign patent documents and non-patent literature in accordance with 37 C.F.R. 1.98(a)(2).

Respectfully submitted,

LEONARD FORBES ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A. P.O. Box 2938
Minneapolis, MN 55402
(612) 373-6960

Date 5-10-04

3y <u>//</u>

Marvin L. Beekman Reg. No. 38,377

<u>CERTIFICATE UNDER 37 CFR 1.8:</u> The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this **1071** day of May, 2004.

Signature

Substitute for form 1449A/PTO Complete if Known INFORMATION DISCLOSURE **Application Number** 10/623788 STATEMENT BY APPLICANT (Use as many sheets as necessary) July 21, 2003 Filing Date Forbes, Leonard **First Named Inventor Group Art Unit** 2811 Unknown **Examiner Name** Attorney Docket No: 1303.109US1 Sheet 1 of 7

		US P	ATENT DOCUMENT	S		
Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	Filing Date If Appropriate
	US- 2002/0001965	01/03/2002	Forbes, Leonard	438	734	07/22/1997
	US- 2002/0070421	06/13/2002	Ashburn, Stanton P.	257	510	02/08/2002
	US- 2003/0227072	12/11/2003	Forbes, Leonard	257	616	06/10/2002
	US-4,241,359	12/23/1980	Izumi, Katsutoshi , et al.	257	386	03/02/1978
	US-4,314,595	02/09/1982	Yamamoto, et al.	148	1.5	01/08/1980
	US-4,589,928	05/20/1986	Dalton, John V.	438	142	08/21/1984
	US-5,426,061	06/20/1995	Sopori, Bhushan L.	438	475	09/06/1994
	US-5,661,044	08/26/1997	Holland, Orin W., et al.	438	766	06/15/1995
	US-5,840,590	11/24/1998	Myers Jr., Samuel M., et al.	438	471	12/01/1993
	US-5,879,996	03/09/1999	Forbes, Leonard	438	289	09/18/1996
	US-5,963,817	10/05/1999	Chu, Jack O., et al.	438	410	10/16/1997
	US-6,022,793	02/08/2000	Wijaranakula, Witawat , et al.	438	473	10/21/1997
	US-6,083,324	07/04/2000	Henley, Francois J., et al.	148	33.2	02/19/1998
	US-6,093,623	07/25/2000	Forbes, Leonard	438	455	08/04/1998
	US-6,174,784	01/16/2001	Forbes, Leonard	438	405	11/14/1997
	US-6,204,145	03/20/2001	Noble, Wendell P.	438	412	08/07/1998
	US-6,228,694	05/08/2001	Doyle, Brian S., et al.	438	199	06/28/1999
,	US-6,251,751	06/26/2001	Chu, Jack O., et al.	438	439	04/13/1999
	US-6,261,876	07/17/2001	Crowder, S. W., et al.	438	149	11/04/1999
	US-6,309,950	10/30/2001	Forbes, Leonard	438	455	03/23/2000
	US-6,315,826	11/13/2001	Muramatsu, Satoru	117	95	06/22/2000
	US-6,338,805	01/15/2002	Anderson, Gary L.	216	89	07/14/1999
	US-6,339,011	01/15/2002	Gonzalez, Fernando , et al.	438	473	03/05/2001
	US-6,377,070	04/23/2002	Forbes, Leonard	326	41	02/09/2001
	US-6,383,924	05/07/2002	Farrar, Paul A., et al.	438	667	12/13/2000
	US-6,424,001	07/23/2002	Forbes, Leonard, et al.	257	315	02/09/2001
	US-6,448,601	09/10/2002	Forbes, Leonard, et al.	257	302	02/09/2001
	US-6,461,933	10/08/2002	Houston, T. W.	438	423	11/08/2001

Substitute for form 1449A/PTO	Under the Paparwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid UNIS control number. Complete if Known		
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)	Application Number	10/623788	
	Filing Date	July 21, 2003	
	First Named Inventor	Forbes, Leonard	
	Group Art Unit	2811	
	Examiner Name	Unknown	
Sheet 2 of 7	Attorney Docket No: 1	303.109US1	

US-6,478,883	11/12/2002	Tamatsuka, Masaro , et al.	148	33.2	04/18/2000
US-6,496,034	12/17/2002	Forbes, Leonard, et al.	326	041	02/09/2001
US-6,531,727	03/11/2003	Forbes, Leonard, et al.	257	302	02/09/2001
US-6,538,330	03/25/2003	Forbes, Leonard	257	777	03/23/2000
US-6,541,356	04/01/2003	Fogel, K. E., et al.	438	480	05/31/2001
US-6,559,491	05/06/2003	Forbes, Leonard, et al.	257	296	02/09/2001
US-6,566,682	05/20/2003	Forbes, Leonard	257	51	02/09/2001
US-6,582,512	06/24/2003	Geusic, Joseph E., et al.	117	3	05/22/2001
US-6,583,437	06/24/2003	Mizuno, T., et al.	257	19	03/19/2001
US-6,597,203	07/22/2003	Forbes, Leonard	326	98	03/14/2001
US-6,649,476	11/18/2003	Forbes, Leonard	438	268	02/15/2001

	FOREIGN PATENT DOCUMENTS					
Examiner Initials*	Printication Hate					
	EP-434984	09/03/1991	Lindberg, Keith J., et al.	H01L	21/322	

	OTHER	R DOCUMENTS NON PATENT LITERATURE DOCUMENTS	
Examiner Initials*	Cite No 1	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T²
		"Cornell Demonstrates a Universal Substrate", Compound Semiconductor, 3(2), (March/April 1997),27-29	
		ABE, T, "Silicon Wafer-Bonding Process Technology for SOI Structures", Extended Abstracts of the 22nd (1990 International) Conference on Solid State Devices and Materials, (1990),853-856	
		AUBERTON-HERVE, A J., "SOI: Materials to Systems", International Electron Devices Meeting. Technical Digest, (1996),3-10	
		AUTUMN, KELLAR, et al., "Adhesive force of a single gecko foot-hair", Nature, 405(6787), (June 2000),681-685	
		AUTUMN, KELLAR, et al., "Evidence for van der Waals adhesion in gecko setae.", Proceedings of the National Academy of Science U S A.; 99(19), (September 17, 2002),12252-6	
		BAGINSKI, T. A., "Back-side germanium ion implantation gettering of silicon", Journal of the Electrochemical Society, 135(7), Dept of Electrical Engineering, Auburn Univ, AL,(July 1988),1842-3	
		BELFORD, RONA E., et al., "Performance-Augmented CMOS Using Back-End Uniaxial Strain", IEEE 60th DRC. Conference Digest Device Research Conference, 2002, (June 24-26, 2002),41-42	

EXAMINER

DATE CONSIDERED

PTO/SB/08A(10-01)
Approved for use through 10/31/2002, OMB 651-0031
US Patent & Trademerk Office: U.S. DEPARTMENT OF COMMERCE
on of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO	Complete if Known			
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Application Number	10/623788		
(Use as many sheets as necessary)	Filing Date	July 21, 2003		
	First Named Inventor	Forbes, Leonard		
	Group Art Unit	2811		
	Examiner Name	Unknown		
	Attornov Docket No. 1	1202 1001 161		
Sheet 3 of 7	Attorney Docket No: 1303.109US1			

	OTHE	R DOCUMENTS NON PATENT LITERATURE DOCUMENTS	
Examiner Initials*	Cite No 1	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T²
		BERTI, M., "Composition and Structure of Si-Ge Layers Produced by Ion	
		Implantation and Laser Melting", Journal of Materials Research, 6(10), (October	
		1991),2120-2126	
		BERTI, M., "Laser Induced Epitaxial Regrowth of Si ₁ - _x Ge _x /Si Layers Produced	
		by Ge Ion Implantation", Applied Surface Science, 43, (1989),158-164	ļ
		BIALAS, F., et al., "Intrinsic Gettering of 300 mm CZ Wafers", Microelectronic	
		Engineering, 56(1-2), (May 2001),157-63	
		BIEVER, CELESTE, "Secret of 'strained silicon' revealed: behind closed doors,	
		Intel has perfected a novel way to improve chip performance.", New Scientist, 180(i2426-2428), (December 20, 2003),27	
		BINNS, M. J., et al., "The Realization of Uniform and Reliable Intrinsic Gettering	
		in 200mm P- & P/P Wafers for a Low Thermal Budget 0.18 mu m Advanced	
		CMOS Logic Process", <u>Diffusion and Defect Data Pt.B: Solid State Phenomena</u> ,	
		<u>82-84,</u> (2001),387-92	<u> </u>
		BRONNER, G. B., et al., "Physical Modeling of Backside Gettering", Impurity	
		<u>Diffusion and Gettering in Silicon Symposium,</u> Sponsor: Mater. Res. Soc, Nov	
		1984, Boston, MA,(1985),27-30	ļ
		BROWN, CHAPPELL, "Bonding twist hints at universal substrate", <u>EETimes</u> ,	
		(1997),2 pages	<u> </u>
		BRUEL, M, et al., "Smart-Cut: a new silicon on insulator material technology	
		based on hydrogen implantation and wafer bonding", <u>Japanese Journal of</u>	
		Applied Physics, Part 1 (Regular Papers, Short Notes & Review Papers), 36(3B),	
		(1997),1636-1641	 -
		CHEN, XIANGDONG, et al., "Vertical P-MOSFETs with heterojunction between source/drain and channel", IEEE Device Research Conference, (2000),25-26	
		CHILTON, B T., et al., "Solid phase epitaxial regrowth of strained Si ₁ — _x Ge _x /Si	
		strained-layer structures amorphized by ion implantation", Applied Physics	
		<u>Letters, 54(1),</u> (January 2, 1989),42-44	ļ
-		CHOE, K. S., et al., "Minority-Carrier Lifetime Optimization in Silicon MOS	
:		Devices by Intrinsic Gettering", <u>Journal of Crystal Growth, 218(2-4)</u> , (September 2000),239-44	
		CLARK, DON, et al., "Intel unveils tiny new transistors: Process handles circuits	
		1/2000th the width of a human hair", The Wall Street Journal, (August 13,	
		2002),3 pages	
		CLIFTON, P.A., et al., "A process for strained silicon n-channel HMOSFETs",	
		ESSDERC'96. Proceedings of the 26th European Solid State Device Research	
		Conference, (September 1996),519-22	<u>L</u> _
		DUBBELDAY, W B., et al., "Oscillatory strain relaxation in solid phase epitaxially	
		regrown silicon on sapphire", Proceedings of the First International Workshop	
		Lattice Mismatched Thin Films, (September 13-15, 1998),13-17	

PTO/SB/08A(10-01)
Approved for use through 10/31/2002, OAIB 651-0031
US Patant & Trademark Office: U.S. DEPARTMENT OF COMMERCE
tion of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO	Complete if Known			
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)	Application Number	10/623788		
	Filing Date	July 21, 2003		
	First Named Inventor	Forbes, Leonard		
	Group Art Unit	2811		
	Examiner Name	Unknown		
Sheet 4 of 7	Attorney Docket No: 1303.109US1			

 	OTHE	R DOCUMENTS NON PATENT LITERATURE DOCUMENTS	
Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T²
		FISCHETTI, M V., et al., "Band structure, deformation potentials, and carrier	
		mobility in strained Si, Ge, and SiGe alloys", <u>Journal of Applied Physics</u> , 80(4),	
		(August 15, 1996),2234-2252	<u> </u>
		FOURNEL, F, et al., "Ultra High Precision Of The Tilt/Twist Misorientation	
		Angles In Silicon/Silicon Direct Wafer Bonding", <u>Abstract - Electronic Materials</u> Conference, (June 2002),9	
		GARCIA, G A., et al., "High-quality CMOS in thin (100 nm) silicon on sapphire",	-
		IEEE Electron Device Letters, 9(1), (January 1988),32-34	
		GODBOLE, H., et al., "An Investigation of Bulk Stacking Faults in Silicon Using	
İ		Photocapacitance Transient Spectroscophy", Materials Letters, 8(6-7), Dept of	
		Electr & Comput Engr, Oregon State Univ, Corvallis OR,(July 1989),201-3	
		GONG, S. S., et al., "Implantation Gettering in Silicon", Solid-State Electronics,	
		30(2), (February 1987),209-11	
		GRAF, D., et al., "300 mm epi pp- wafer: is there sufficient gettering?", High	
		Purity Silicon VI. Proceedings of the Sixth International Symposium	
		(Electrochemical Society Proceedings Vol. 2000-17) (SPIE Vol.4218),	
		(2000),319-30	ļ
		HADDAD, H., et al., "Carbon Doping Effects on Hot Electron Trapping", 28th	
		Annual Proceedings. Reliability Physics 1990, (March 1990),288-9	
		HADDAD, H., et al., "Electrical Activity of Bulk Stacking Faults in Silicon",	
		Materials Letters, 7(3), Hewlett-Packard Northwest Integrated Circuits Div,	
		Corvallis OR,(September 1988),99-101	ļ
		IYER, S.S., "Separation by Plasma Implantation of Oxygen (SPIMOX)	
		operational phase space", <u>IEEE trans. on Plasma Science, 25,</u> (1997),1128- 1135	
		KALAVADE, PRANAV, et al., "A novel sub-10 nm transistor", 58th DRC. Device	
		Research Conference Conference Digest, (June 19-21, 2000),71-72	
		KANG, J. S., et al., "Gettering in Silicon", Journal of Applied Physics, 65(8).	
İ		Center for Solid State Electron Res., Arizona State Univ., Tempe, AZ,(April 15,	
		1989),2974-85	<u> </u>
		KOSTRZEWA, M, et al., "Testing the Feasibility of strain relaxed InAsP and	
		InGaAs compliant substrates", EMC 2003 International Conference Indium	
		Phosphide and Related Materials. Conference Proceedings, Other authors: G.	
		Grenet et al,(6/2003),8-9	<u> </u>
		KUNG, C. Y., et al., "The effect of carbon on oxygen precipitation in high carbon	
		CZ silicon crystals", Materials Research Bulletin, 18(12), Silicon Materials Div.,	
		Fairchild Camera & Instrument Corp, Healdsburg, CA,(December 1983),1437-41	1
		LASKY, J. B., "Wafer Bonding for Silicon-on-Insulator Technologies", <u>Applied</u> Physics Letters, 48(1), (January 6, 1986),78-80	
		1 11/5/05 25/075, 40(1), (balldary 0, 1000),10-00	

PTO/SB/08A(10-01)
Approved for use through 10/31/2002, OMB 651-0031
US Patent & Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid CMS control number.

Substitute for form 1449A/PTO	Complete if Known			
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Application Number	10/623788		
(Use as many sheets as necessary)	Filing Date	July 21, 2003		
	First Named Inventor	Forbes, Leonard		
	Group Art Unit	2811		
	Examiner Name	Unknown		
Sheet 5 of 7	Attorney Docket No: 1303.109US1			

	OTHER	R DOCUMENTS NON PATENT LITERATURE DOCUMENTS	
Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T²
		LI, Y. X., et al., "New intrinsic gettering process in Czochralski-silicon wafer", 6th	
		International Conference on Solid-State and Integrated Circuit Technology.	İ
		<u>Proceedings, 1(1), (2001),277-9</u>	
		LOO, Y L., et al., "Contact Printing With Nanometer Resolution", Device	
		Research Conference, (June 2002),149-150	
		LU, D, , "Bonding Silicon Wafers by Use of Electrostatic Fields Followed by	
		Rapid Thermal Heating", Materials Letters, 4(11), (October 1986),461-464	
		MIZUNO, T, et al., "Advanced SOI-MOSFETs with Strained-Si Channel for High	
		Speed CMOS Electron/Hole Mobility Enhancement", 2000 Symposium on VLSI	
		Technology. Digest of Technical Papers, (2000),210-211	ļ.,.
		MORAN, PETER, "Strain Relaxation in Wafer-Bonded SiGe/Si Heterostructures	
		Due to Viscous Flow of an Underlying Borosilicate Glass", Electronic Materials	
		Conference, Santa Barbara, June 2002, Abstract, (June 2002), Pgs. 8-9	
		MUMOLA, P. B., et al., "Recent advances in thinning of bonded SOI wafers by	
-		plasma assisted chemical etching", Proceedings of the Third International	
		Symposium on Semiconductor Wafer Bonding: Physics and Applications,	
		(1995),28-32	ļ
		NAYAK, D.K., "High performance GeSi quantum-well PMOS on SIMOX",	ļ
		International Electron Devices Meeting 1992. Technical Digest, (1992),777-80	<u> </u>
		NICHOLS, F A., "Surface-(inteface) and volume-diffusion contributions to	
		morphological changes driven by capillarity", <u>Transactions of the American</u>	
		Institute of Mining, Metallurgical and Petroleum Engineers, 233(10),	İ
		(1965),1840-8	ļ <u>-</u> -
		O'NEILL, A G., et al., "High speed deep sub-micron MOSFET using high mobility	
1		strained silicon channel", ESSDERC '95. Proceedings of the 25th European	
		Solid State Device Research Conference, (September 1995), 109-12	ļ
i		OMI, HIROO, et al., "Semiconductor Surface with Strain Control",	
	·	http://www.brl.ntt.co.jp/J/kouhou/katsudou/report00/E/report04_e.html,	
		OR, B S., et al., "Annealing effects of carbon in n-channel LDD MOSFETS",	
		IEEE Electron Device Letters, 12(11), Dept of Electrical & Computing Engr,	
		Oregon State Univ, Corvallis OR,(November 1991),596-8	
		OUYANG, Q, et al., "Bandgap Engineering in Deep Submicron Vertical	
		pMOSFETs", IEEE 58th DRC. Device Research Conference. Conference Digest,	
		(2000),27-28	-
		PAINE, D. C., "The Growth of Strained Si ₁ - xGe _x Alloys on <001> Silicon Using	1
		Solid Phase Epitaxy", <u>Journal of Materials Research</u> , 5(5), (May 1990),1023-1031	
	 	PEOPLE, R., "Calculation of critical layer thickness versus lattice mismatch for	+
		$Ge_xSi_1 - x/Si$ strained-layer heterostructures", Applied Physics Letters, 47(3),	
		(August 1, 1985),322-4	
		(August 1, 1000),022-4	
		<u> </u>	

PTO/SB/08A(10-01)
Approved for use through 10/31/2002, OMB 651-0031
US Patent & Trademark Office: U.S. DEPARTMENT OF COMMERCE
on of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO	Complete if Known		
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Application Number	10/623788	
(Use as many sheets as necessary)	Filing Date	July 21, 2003	
	First Named Inventor	Forbes, Leonard	
	Group Art Unit	2811	
	Examiner Name	Unknown	
Sheet 6 of 7	Attorney Docket No: 1	303.109US1	

	OTHE	R DOCUMENTS NON PATENT LITERATURE DOCUMENTS	
Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T²
		RIM, KERN, et al., "Fabrication and analysis of deep submicron strained-Si n-MOSFET's", <u>IEEE Transactions on Electron Devices</u> , <u>47(7)</u> , (July 2000),1406-1415	
		RIM, KERN, et al., "Strained Si NMOSFETs for High Performance CMOS Technology", 2001 Symposium on VLSI Technology. Digest of Technical Papers, (2001),59-60	
		RIM, KERN, et al., "Transconductance enhancement in deep submicron strained Si n-MOSFETs", <u>International Electron Devices Meeting 1998.</u> Technical Digest, (1998),707-710	
		RUBIN, L, et al., "Effective gettering of oxygen by high dose, high energy boron buried layers", 1998 International Conference on Ion Implantation Technology. Proceedings, 2(2), (1998),1010-13	
		SATO, TSUTOMU, "A New Substrate Engineering for the Formation of Empty Space in Silicon (ESS) Induced by Silicon Surface Migration", <u>IEDM Digest</u> , paper 20.6.1, (1999),20.6.1-20.6.4	
		SATO, T, "Trench transformation technology using hydrogen annealing for realizing highly reliable device structure with thin dielectric films", 1998 Symposium on VLSI Technology Digest of Technical Papers, (1998),206-7	
		SUGIYAMA, N, et al., "Formation of strained-silicon layer on thin relaxed-SiGe/SiO/sub 2//Si structure using SIMOX technology", Thin Solid Films, 369(1-2), (July 2000),199-202	
		TAKAGI, SHIN-ICHI, "Strained-Si- and SiGe-On-Insulator (Strained-SOI and SGOI) MOSFETs for High Performance/Low Power CMOS Application", <u>IEEE Device Research Conference</u> , 2002. 60th DRC. Conference Digest, (2002),37-40	
		TAN, T. Y., et al., "Intrinsic Gettering by Oxide Precipitate Induced Dislocations in Czochralski Silicon", <u>Applied Physics Letters</u> , Vol 30, No. 4, (February, 1977),175-176	
		VERDONCKT-VANDEBROEK,, SOPHIE, et al., "SiGe-Channel Heterojunction p-MOSFET's", IEEE Transactions on Electron Devices, 41(1), (January 1994),90-101	
		WELSER, J, et al., "Strain dependence of the performance enhancement in strained-Si n-MOSFETs", <u>IEEE International Electron Devices Meeting 1994.</u> <u>Technical Digest</u> , (December 11-14, 1994),373-376	
		WHITWER, F. D., et al., "DLTS characterization of precipitation induced microdefects", Materials Issues in Silicon Integrated Circuit Processing Symposium, (April 1986),53-57	
		WIJARANAKULA, W., et al., "Effect of Pre- and Postepitaxial Deposition Annealing on Oxygen Precipitation in Silicon", <u>Journal of Materials Research</u> , <u>1(5)</u> , Dept of Electr & Comput Eng, Oregon State Univ, Corvallis, OR,(September-October 1986),698-704	

PTC/SB/08A(10-01)
Approved for use through 10/31/2002, OMB 651-0031
US Patent & Trademark Office: U.S. DEPARTMENT OF COMMERCE
on of information unless it contains a valid OMB control number.

Substitute for form 1449A/PTO	Complete if Known	18qual to 1 espons to a consecution in north second resident contains a feature of the contains
INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Application Number	10/623788
(Use as many sheets as necessary)	Filing Date	July 21, 2003
	First Named Inventor	Forbes, Leonard
	Group Art Unit	2811
	Examiner Name	Unknown
Sheet 7 of 7	Attorney Docket No: 1	1303.109US1

·	OTHER	R DOCUMENTS NON PATENT LITERATURE DOCUMENTS	
Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		WIJARANAKULA, W., et al., "Effect of preanneal heat treatment on oxygen precipitation in epitaxial silicon", <u>Materials Issues in Silicon Integrated Circuit Processing Symposium</u> , (April 1986),139-44	
		WIJARANAKULA, W., et al., "Internal Gettering Heat Treatments and Oxygen Precipitation in Epitaxial Silicon Wafers", <u>Journal of Materials Research</u> , 1(5), Dept of Electr & Comput. Eng, Oregon State Univ., Corvallis, OR,(September-October 1986),693-7	
		WIJARANAKULA, W., et al., "Oxygen precipitation in p/p+(100) epitaxial silicon material", <u>Journal of the Electrochemical Society</u> , 134(9), SEH America, Inc., Mater. Characterization Lab., Vancouver, WA,(September 1987),2310-16	
		WILD, DIPL.ING. M., "Laser Assisted Bonding of Silicon and Glass in Micro-System Technology", http://www.ilt.fhg.de/eng/jb00-s42.html , Fraunhofer ILT - jb00-s42,(2003),1	
		XUAN, PEIQI, et al., "60nm Planarized Ultra-thin Body Solid Phase Epitaxy MOSFETs", IEEE Device Research Conference, Conference Digest. 58th DRC, (June 19-21, 2000),67-68	
:		YANG, D., et al., "Intrinsic Gettering in Nitrogen Doped Czochralski Crystal Silicon", High Purity Silicon VI. Proceedings of the Sixth International Symposium (Electrochemical Society Proceedings Vol. 2000-17) (SPIE Vol.4218), (2000),357-61	
	,	YANG, DEREN, et al., "Nitrogen in Czochralski Silicon", 2001 6th International Conference on Solid-State and Integrated Circuit Technology. Proceedings, 1(1), (2001),255-60	
		YIN, HAIZHOU, "High Ge-Content Relaxed Si ₁ – _x Ge _x Layers by Relaxation on Complaint Substrate with Controlled Oxidation", <u>Electronic Materials Conference</u> , <u>Santa Barbara</u> , <u>June 2002</u> , (June 2002),8	
		ZHU, Z H., et al., "Wafer bonding and its application on compliant universal (CU) substrates", Conference Proceedings, 10th Annual Meeting IEEE Lasers and Electro-Optics Society, (November 10-13, 1996),31	
		ZHU, Z H., et al., "Wafer bonding technology and its applications in optoelectronic devices and materials", <u>IEEE Journal of Selected Topics in Quantum Electronics</u> , (June 1997),927 - 936	